CLAIMS

What is claimed is:

1. A cell protection circuit, comprising:

a transistor coupled to said cell; and

a current bypass device coupled to said transistor and said cell;

wherein said transistor limits the current that can flow through said cell when the voltage across said cell falls to a predetermined minimum level.

2. The cell protection circuit of claim 1 wherein said current bypass device conducts current when said transistor limits the current through the cell.

3. The cell protection circuit of claim 1 wherein said transistor is connected in series with said cell and said current bypass device is connected in parallel to said serially connected transistor and cell.

4. The cell protection circuit of claim 1 wherein said current bypass device comprises a diode.

5. The cell protection circuit of claim 1 wherein said transistor comprises a MOSFET.

6. The cell protection circuit of claim 1 wherein said transistor comprises an n-channel enhancement mode MOSFET.

7. The cell protection circuit of claim 6 wherein the n-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

8. The cell protection circuit of claim 7 wherein said current bypass device comprises a diode.

9. The cell protection circuit of claim 8 wherein said n-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the negative terminal of said cell, said drain terminal couples to the anode of said diode, and the cathode of said diode and said gate terminal couple to the positive terminal of said cell.

10. The cell protection circuit of claim 1 wherein said transistor comprises an p-channel enhancement mode MOSFET.

11. The cell protection circuit of claim 10 wherein the p-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

12. The cell protection circuit of claim 11 wherein said current bypass device comprises a diode.

13. The cell protection circuit of claim 12 wherein said p-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the positive terminal of said cell, said drain terminal couples to the cathode of said diode, and the anode of said diode and said gate terminal couple to the negative terminal of said cell.

14. The cell protection circuit of claim 1 further including a delay device coupled to said cell and said transistor, said delay device slows the rate of change of voltage across said cell with changes in current load on said cell.

15. The cell protection circuit of claim 14 wherein said delay device comprises a resistor coupled to a capacitor.

16. A protection circuit for a cell, comprising:

a means for limiting current through said cell when the voltage across said cell reaches a predetermined threshold; and

a means for conducting current around said cell when the voltage across said cell reaches the predetermined threshold.

17. The protection circuit of claim 16 further including a means for providing a time delay.

18. A method of protecting a cell, comprising:

(a) limiting the current said cell when the voltage across said cell falls to a minimum predetermined level; and

(b) when limiting the current, permitting current to conduct through a bypass device coupled in parallel with said cell.

19. The method of claim 18 wherein (a) is performed using a transistor.

20. The method of protecting a cell further including providing a time delay to the voltage across said transistor.

21. A battery, comprising:

a plurality of cells connected in series; and

a separate protection unit coupled to each cell, each protection unit protecting its associated cell and comprising:

a transistor coupled to said associated cell; and

a current bypass device coupled to said transistor and said associated cell;

wherein said transistor limits the current that can flow through said associated cell when the voltage across said associated cell falls to a predetermined minimum level.

22. The battery of claim 21 wherein said current bypass device conducts current when said transistor limits the current through the cell.

23. The battery of claim 21 wherein said transistor is connected in series with said cell and said current bypass device is connected in parallel to said serially connected transistor and cell.

24. The battery of claim 21 wherein said current bypass device comprises a diode.

25. The battery of claim 21 wherein said transistor comprises a MOSFET.

26. The battery of claim 21 wherein said transistor comprises an n-channel enhancement mode MOSFET.

27. The battery of claim 26 wherein the n-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

28. The battery of claim 27 wherein said current bypass device comprises a diode.

29. The battery of claim 28 wherein said n-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the negative terminal of said cell, said drain terminal couples to the anode of said diode, and the cathode of said diode and said gate terminal couple to the positive terminal of said cell.

30. The battery of claim 21 wherein said transistor comprises an p-channel enhancement mode MOSFET.

31. The battery of claim 30 wherein the p-channel enhancement mode MOSFET has a threshold voltage substantially the same as the predetermined minimum level.

32. The battery of claim 31 wherein said current bypass device comprises a diode.

33. The battery of claim 32 wherein said p-channel enhancement mode MOSFET has gate, source and drain terminals and said source terminal couples to the positive terminal of said cell,

said drain terminal couples to the cathode of said diode, and the anode of said diode and said gate terminal couple to the negative terminal of said cell.

34. The battery of claim 21 further including a delay device coupled to said cell and said transistor, said delay device slows the rate of change of voltage across said cell with changes in current load on said cell.

35. The battery of claim 34 wherein said delay device comprises a resistor coupled to a capacitor.

36. A battery cell protection circuit, comprising:

a current limiter capable of being coupled to a battery cell; and

a bypass device coupled in parallel with the current limiter and cell;

wherein the current limiter functions to limit current to the cell when the cell voltage reaches a predetermined threshold.

37. The circuit of claim 36 wherein the current limiter comprises a transistor.

38. The circuit of claim 36 wherein the current limiter comprises an n-channel MOSFET.

39. The circuit of claim 36 wherein the current limiter comprises a p-channel MOSFET.

40. The circuit of claim 36 wherein the bypass device comprises a diode.

41. The circuit of claim 36 further including a delay element coupled to said current limiter to delay the current limiting action of said current limiter when the cell voltage reaches the predetermined threshold.